CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A recessed channel CMOS device comprising:

an SOI layer having a recessed channel region and adjoining extension implant regions; and

at least one gate region present atop said SOI layer, wherein said adjoining extension implant regions have an abrupt lateral profile and are located beneath said gate region.

2. The recessed channel CMOS of Claim 1 wherein said SOI layer is part of an SOI structure.

3. The recessed channel CMOS of Claim 1 wherein said recessed channel region has a thickness of from about 5 to about 20 nm.

4. The recessed channel CMOS of Claim 1 wherein said SOI layer further comprises source/drain regions.

5. The recessed channel CMOS of Claim 1 wherein said gate region comprises a gate dielectric and a gate conductor.

6. The recessed channel CMOS of Claim 5 wherein said gate dielectric comprises SiO_2, Si_3N_4, SiON, TiO_2, Al_2O_3, ZrO_2, Ta_2O_5, La_2O_5 or any combination thereof.

7. The recessed channel CMOS of Claim 5 wherein said gate conductor comprises polysilicon, an elemental conductive metal, an alloy that includes at least an elemental

conductive metal, a silicide of an elemental conductive metal, a nitride of an elemental conductive metal or any combination thereof.

8. The recessed channel CMOS of Claim 1 further comprising halo implant regions that have an abrupt lateral profile which are located beneath said gate region.

9. The recessed channel CMOS of Claim 1 further comprising permanent spacers present on exposed sidewalls of said gate region.

10. A method of fabricating a recessed channel CMOS device comprising the step of:

providing a patterned oxide layer over an SOI layer, said patterned oxide layer exposing a portion of said SOI layer;

thinning the exposed portion of the SOI layer to form a recessed channel region;

forming a gate dielectric on said recessed channel region;

forming sacrificial nitride spacers on portions of said gate dielectric so as to protect exposed walls of said SOI layer and said oxide layer and forming a gate conductor on other portions of the gate dielectric not containing said sacrificial nitride spacers;

recessing the oxide layer exposing SOI layer abutting the recessed channel region;

forming source/drain diffusion regions in said exposed SOI layer abutting the recessed channel region; and

removing the sacrificial nitride spacers and forming extension implant regions in said SOI layer such that said extension implant regions have an abrupt lateral profile and are located beneath the gate conductor.

11. The method of Claim 10 wherein said thinning is carried out by chemical downstream etching, reactive-ion etching, or thermal oxidation and etching.

12. The method of Claim 10 wherein said thinning is carried out by thermal oxidation and a chemical oxide removal (COR) process.

13. The method of Claim 12 wherein said COR process is carried out at relatively low pressures of 6 millitorr or less and in a vapor of HF and NH_3.

14. The method of Claim 10 wherein said source/drain diffusion regions are formed by ion implantation and annealing.

15. The method of Claim 10 wherein said source/drain extension and halo implant regions are formed by angled implantation and annealing.

16. The method of Claim 10 further comprising forming permanent spacers on exposed sidewalls of said gate conductor and said gate dielectric.

17. The method of Claim 10 wherein said gate conductor is a polysilicon gate conductor that is formed by deposition and ion implantation.

18. The method of Claim 10 further comprising forming trench isolation regions in said SOI layer.

19. The method of Claim 10 further comprising forming halo implant regions after forming said extension implant regions, said halo implant regions having an abrupt lateral profile which are located beneath said gate conductor.

20. The method of Claim 19 wherein said halo implant regions are formed by angled implantation and annealing.